ABSTRACT

In a signal processor according to the present invention, as shown in figure 1, error correction is performed on data which has been subjected to predetermined signal processing, for each predetermined block unit, by an error correction block 152, in parallel with the operation of sequentially storing the data in a cache memory 16. Then, error detection is performed on the data for each predetermined block unit by a descrambling/error detection block 153, and the data is stored in a buffer memory 14. Based on the results of the error detection and the error correction, when there exists some error in the data, the data with the error, which is stored in th e buffer memory 14, is read out to be subjected to error correction again. When there is no error, the data corresponding to one block and stored in the buffer memory 14 is transmitted to a host computer 13 without performing error correction again.